

GENERAL DESCRIPTION

The Xelic Optical Transport Network (OTN) Framers Core (XCO2) performs Optical Channel Transport Unit (OTU), Optical Channel Data Unit (ODU), and Optical Channel Payload Unit (OPU) overhead processing, aligns incoming OTU or ODU frames, and provides overhead interpretation with error detection and performance monitoring. The XCO2 contains independent transmit and receive processors with external ports for overhead insertion and extraction. External ports are provided for optional EFEC processing. System side data is transferred at a nominal rate of 9.953Gb/s using a 64-bit data bus operating at 155.52Mb/s. Line side data is transferred at an OTU2 rate using a 64-bit data bus operating at 167.33Mb/s or at an ODU2 rate using a 64-bit data bus operating at 156.83Mb/s.

The XCO2 Transmit Processor inserts OTU2, ODU2, and OPU2 overhead, calculates and inserts parity, automatically generates Backward Defect Indication (BDI) signaling, and scrambles generated frames. Support is provided for up to 6 levels of tandem connection overhead insertion. Programmable Trail Trace Identifier buffers are implemented for Section Monitoring (SM), Path Monitoring (PM), and Tandem Connection Monitoring overhead insertion. Diagnostics support includes optional corruption of inserted parity, corruption of scrambling, frame alignment signal corruption, and maintenance signal insertion. Programmable payload support includes asynchronous CBR10G, bit synchronous CBR10G, ATM, GFP, null test, and PRBS mapping types. Forward Error Correction (FEC) encoding is provided for generated OTU2 frames using Reed Solomon RS(255,239) 16 byte interleaved codes. ODU2 frames are optionally generated through programmable register control.

The XCO2 Receive Processor contains a configurable frame alignment unit with programmable options for OOF/OOM and LOF/LOM algorithm state transitions. Incoming OTU or ODU frames are descrambled (optional) and aligned for OTN overhead processing. OTU, ODU, and OPU overhead information is extracted to both internal register locations and an external overhead port. Frame alignment signal overhead is interpreted to detect and report various conditions which include OOF, LOF, LOA, OOM, LOM, and LOMA. OTU AIS, ODU AIS, ODU LCK, ODU OCI and client generic AIS maintenance signals are detected with optional interrupt generation. OPU payload type mismatch error conditions are detected and support is provided for programmable payload type accept and inconsistent thresholds. A configurable output is provided to indicate FEC bit error rate detection of 10^{-3} or 10^{-4} .

Performance counters (configurable for bit or block count type) are provided for the accumulation of inserted (XCO2 transmit processor) and detected (XCO2 receive processor) positive and negative justification events along with BIP-8 parity and BEI errors for OTU SM, ODU TCMi, and ODU PM (XCO2 receive processor). Counters are configurable

for saturating latch and clear operation or periodic error sync auto-update mode.

The XCO2 provides facility and terminal loopback modes of operation using Transmit and Receive Processor data path configurations for system debug purposes.

A 16-bit generic register interface for access and configuration of internal memory mapped locations is included.

FEATURES

- Suitable for FPGA and/or ASIC implementations.
- Integration support and maintenance available.
- XCO2 core available under flexible single use licensing terms with netlist or source code deliverables.
- Implements flexible data bus architecture.
- Provides for streaming and normal modes of operation.
- Implements 16-bit register interface for programming of internal registers.
- Complies with ITU-T G.709 and ITU-T G.798 specifications.
- Supports transmit and receive facility and terminal loopback configurations.
- Accepts streaming ODU2 frames or mapped client signals which include synchronous or asynchronous CBR10G, ATM, GFP, and non specific client bit streams.
- Flexible insertion and extraction of OTU, ODU, and OPU overhead byte information.
- Supports corruption capability through internal register programming for debug or test purposes.
- Inserts OTU2 or ODU2 frame alignment signal information with a programmable corruption option.
- Provides optional scrambling $(1 + x + x^3 + x^{12} + x^{16})$ with polynomial corruption capability for diagnostics.
- Inserts OTU SM, GCC0, and RES overhead through internal register control or an external overhead port.
- Inserts ODU RES, TCM ACT, FTFL, PM, EXP, GCC1, GCC2, and APS/PCC overhead through internal register control or an external overhead port.
- Provides 6 levels of tandem connection overhead insertion/extraction for both transmit and receive processors.
- Contains external ports for optional EFEC core interfacing.
- Programmable positive and negative justification counters provided for asynchronous CBR payload types with user defined interval or errored second accumulation.
- Optionally inserts OTU AIS, ODU AIS, ODU LCK, ODU OCI and client generic AIS maintenance signals.
- Optional RS(255,239) FEC encoding capability.
- Provides optional descrambling with polynomial corruption capability for diagnostics.
- Performs selectable OTU2 or ODU2 frame alignment with programmable OOF/OOM and LOF/LOM detection.
- Detects FAS OOF, LOF, LOA, OOM, LOM, and LOMA conditions with optional interrupt generation.

- Provides saturating counters with programmable latch and clear or incoming error sync capture configurations.
- Provides independent performance counters for the accumulation of OOF and OOM errors with optional interrupt generation for OOF and OOM error detection.
- Optional RS(255,239) FEC decode capability is provided with correctable and uncorrectable error counts.
- Detects OTU-AIS error condition with optional interrupt generation.
- Interprets and extracts OTU SM, GCC0 and RES overhead information to internal register locations with programmable accept and inconsistent maskable interrupt capability.
- Provides 16-bit performance counters for the accumulation of SM BIP-8 and SM BEI errors with maskable interrupt capability.
- Provides performance counters for the accumulation of FEC correctable symbols, correctable 0's/1's, and uncorrectable error counts with maskable interrupt capability.
- Interprets and extracts ODU RES, TCM ACT, TCM (support for up to 6 levels of tandem connection monitoring), PM, EXP, GCC1, GCC2, and APS/PCC overhead information to internal register locations with programmable accept and inconsistent maskable interrupt capability.
- Provides independent performance counters for the accumulation BIP-8 and BEI errors (SM, TCMi, PM) with optional interrupt generation.

APPLICATIONS

- Traffic Manager
- DWDM and WDM systems
- OTN/SONET add/drop multiplexers
- Digital cross connects
- OTN and/or SONET/SDH line cards
- Test equipment